OMKAR BHILARE

DIGITAL DESIGN AND VERIFICATION ENTHUSIAST

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EDUCATION

Veermata Jijabai Technological Institute *Mumbai, India.*

B.Tech in Electronics Engineering(**CGPA: 9.02**) *August 2018 - April 2022*

- ***Relavant Coursework***: Electronics Circuit Analysis and Design, Digital Combinational Circuits, Digital Sequential Circuits, Microprocessor and Microcontroller, Principle of VLSI, Embedded Systems.

EXPERIENCE

Verification Intern **Mrs.Lavanya J, Prof.V.Kamakoti**

Shakti Lab, RISE Group, IIT Madras *March 2021 - July 2021*

- Designed and developed an **FPGA framework to verify the SHAKTI processors on the FPGAs.**
- Developed a Python Wrapper called *AAPG on FPGA* which automatically generates single and multiple aapg tests which are suitable to run on the FPGA. These tests are random RISC-V programs to verify RISC-V cores.
- OpenOCD and GDB are used for flashing the test program to the Arty A7-100 FPGA which is running a soft-core Vajra SOC. The python wrapper also compares the FPGA's test signature dump with the reference software spike signature dump.
- Proposed work **increased the verification speed while maintaining visibility and control** in the FPGA flow.
- Studied and tested a **cocotb UVM Framework for the verification of SSPI and MBOX** IPs of SHAKTI.
- **Project Report of FPGA Based Verification of Shakti C-Class: *REPORT***

Open Source Developer **Mr.Michael Welling**

Google Summer of Code 2021, BeagleBoard Organization *June 2021 - Aug 2021*

- Built and tested a **Gateware for Beaglewire**(Lattice iCE40 FPGA-cape) for Beaglebone Black.
- **Interfaced AM335x Arm Chip with Lattice FPGA** using protocols like GPMC and Wishbone.
- Designed and verified GPMC to Wishbone converter IP. It supported single read and writes, also included two flop synchronizer to ensure synchronization.
- Developed wishbone slave examples for Beaglewire. Designed 1 Master to N slaves Wishbone Intercon for Beaglewire which were used to test multiple slave condition.
- Interfaced BeagleWire with SDRAM using litedram core which included serv a bit-serial RISC-V CPU for initialization of SDRAM IP.
- Designed a VGA Driver for Beaglewire, tested the design in Hardware with VGA PMOD. Developed a gateware for PONG game and Encoder PMOD for Beaglewire.
- **Software Repository:** *github.com/BeagleWire* **Report of GSoC 2021: *beaglewire.github.io***

R&D Intern **Mr.Nitesh Vasant**

FireFly LED Products Pvt Ltd *May 2019 - July 2019*

- Designed Metal Core Printed Circuit Boards(MCPCBs) using Altium for LED lights with an on-board driver, tested the design with driver ICs from different manufactures.
- Designed and tested an optimal combination of driver IC and LED circuit design which had maximum efficiency.

PROJECTS

RISC-V core github.com/riscv-core

Icarus Verilog, GTKWAVE, Yosys, Openlane, Magic, TD IDE Jan 2021 - March 2021

- Designed a RISC-V core in Verilog which supports R, I type of Instruction.
- Converted basic design into silicon (GDSII) format using Openlane and sky130 Technology.
- Designed FPGA drivers like VGA, Seven Segment for future integration into the core. Tested the drivers on the Tang Primer FPGA.

8 Bit Computer using 74LS series ICs github.com/8-bit-computer
Logisim, Multisim May 2020 - Nov 2020

- Designed an entire 8 Bit Computer circuit using 74LS series ICs and simulated it on Logisim Software.
- Two cascaded 74LS181 used for Arithmetic Logical Unit(ALU) of 8 Bit Computer which can do 8 Bit Arithmetic and Logical operation.

ESP32 based Development board github.com/ESP32-based-dev-board
Eagle, Proteus, Multisim May 2020 - July 2020

- Designed and assembled a double layer ESP32 based board using Autodesk EAGLE. It has peripherals like the motor drivers, buck circuit, over current and reverse voltage protection.
- Tested the PCB using custom variable load and before fabrication simulated sub-circuits of PCB.

SKILLS

FPGAs:	Xilinx's Arty A7-100, Altera's Cyclone II, Lattice's ICE40UP5K & iCE40HX4k, Anlogic's EG4S20.
Languages:	Verilog, VHDL, C, Python, Assembly Language(x86, RISC-V).
EDA Tools:	Quartus Prime, Xilinx Vivado, IceStorm.
Microcontrollers:	ESP32, ESP8266, Atmega328p, AM335x.
Software & Frameworks:	CoCotb, Icarus Verilog, GTKWave, Autodesk Eagle, Altium, Kicad, Proteus, Multisim, Logisim, Git, Linux.

POSITION OF RESPONSIBILITY

Jt. General Secretary **Dr.A.S.Rao**
Society of Robotics and Automation (SRA), VJTI August 2019 - present

- Taught topics like Microcontroller Architecture, Printed Circuit Board Designing, Voltage regulators and PID control in various workshops for over hundred freshmen students.
- Successfully Conducted PCB designing using Autodesk EAGLE and Self Balancing and Line Following Robot workshops for freshmen students of VJTI.
- Served as a Jt. General Secretary of the Society of Robotics and Automation. Also mentored freshmen students for digital and analog electronics projects.

ACHIEVEMENTS

- **BeagleWire Software** project got selected in Google Summer of Code Program. June 2021
- **8 Bit Computer** project got selected under the Summer of Making program by Hack Club. May 2020
- State Rank 1 in diploma Electronics. May 2019
- Gold Medalist, Class of 2019 - Diploma in Electronics, VJTI. May 2019

CO-CURRICULAR ACTIVITIES

- Achieved **91.64 %** in the course **Introduction to FPGA Design for Embedded Systems** offered by the University of Colorado Boulder on Coursera.
- Successfully Conducted PCB designing using Autodesk EAGLE and Self Balancing and Line Following Robot workshops for freshmen students of VJTI.
- Achieved **AA** grade in **Microprocessor and Microcontroller Systems**, **Digital Combinational Circuits** and **Digital Sequential Circuits** in academic courses provided by VJTI.